Ref No:

SRI KRISHNA INSTITUTE OF TECHNOLOGY, BANGALORE

COURSE PLAN

Academic Year 2019-20

Program:	B E – ELECTRONICS AND COMMUNICATION Engineering
Semester :	3
Course Code:	18EC35
Course Title:	COMPUTER ORGANIZATION
Credit / L-T-P:	3 / 3-0-0
Total Contact Hours:	40
Course Plan Author:	Mrs.SYEDA N

Academic Evaluation and Monitoring Cell

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Table of Contents

Note : Remove "Table of Content" before including in CP Book
Each Course Plan shall be printed and made into a book with cover page
Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

A. COURSE INFORMATION

1. Course Overview

Degree:	BE	Program:	EC
Semester:	3	Academic Year:	2019-20
Course Title:	Computer Organisation	Course Code:	18EC35
Credit / L-T-P:	3 / 3-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	60 Hours	SEE Marks:	60 Marks
CIA Marks:	40 Marks	Assignment	1 / Module
Course Plan Author:	Mrs. Syeda N	Sign ..	Dt:
Checked By:		Sign ..	Dt:
CO Targets	CIA Target : ……. %	SEE Target:	……. %

Note: Define CIA and SEE % targets based on previous performance.

2. Course Content

Content / Syllabus of the course as prescribed by University or designed by institute. Identify 2 concepts per module as in G.

Module	Content	Teaching Hours	Identified Module Concepts	Blooms Learning Levels
1	**Basic Structure of Computers:** Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance – Processor Clock, Basic Performance Equation **Machine Instructions and Programs:** Numbers, Arithmetic Operations and Characters, IEEE standard for	8	Computer Organization and Machine instructions structure	L2, L4

	Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing			
2	**Addressing Modes**, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions	8	Input output organization and subroutines and Standard input output interfaces	L2
3	**Input/Output Organization:** Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access	8	Accessing interrupts through different techniques	L2, L4
4	**Memory System:** Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage-Magnetic Hard Disks	8	Memory System and storage devices	L2,L3
5	**Basic Processing Unit:** Some Fundamental Concepts, Execution of a Complete Instruction,Multiple Bus Organization, Hardwired Control, Microprogrammed Control	8	Processing unit and Embedded system and large computer system	L2
-	**Total**	**40**	**-**	**-**

3. Course Material

Books & other material as recommended by university (A, B) and additional resources used by course teacher (C).

1. Understanding: Concept simulation / video ; one per concept ; to understand the concepts ; 15 – 30 minutes
2. Design: Simulation and design tools used – software tools used ; Free / open source
3. Research: Recent developments on the concepts – publications in journals; conferences etc.

Modules	Details	Chapters in book	Availability
A	**Text books (Title, Authors, Edition, Publisher, Year.)**	**-**	**-**
1,2,3,4,5	Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGraw Hill,2002..	1,2,3,4,5, 6,7, 8	In Lib / In Dept
B	**Reference books (Title, Authors, Edition, Publisher, Year.)**	**-**	**-**
1,2,3,	William Stallings: Computer Organization & Architecture, 9 th	1,2	In Lib

4,5	Edition, Pearson, 2015.		
1,2,3,4	David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface ARM Edition, 4th Edition, Elsevier, 2009.	1,2,3,4,5, 7, 8	In Lib
1,2,3,4,5	Vincent P. Heuring& Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.	5	In Lib
C	**Concept Videos or Simulation for Understanding**	**-**	**-**
C1	https://cosmolearning.org/video-lectures/introduction-to-computer-architecture-7917/		
C2	https://www.youtube.com/watch?v=Z6NERIPT440		
C3	https://www.gatevidyalay.com/addressing-modes/		
C4	https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials/		
C5	https://www.youtube.com/watch?v=zaAwvU-sfUI		
C6	https://www.youtube.com/watch?v=-6CQcvUCKXY		
C7	https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials/#mo		
C8	https://www.geeksforgeeks.org/cache-memory-in-computer-organization/		
C9	*https://computersciencewiki.org/index.php/Architecture_of_the_central_processing_unit_(CPU)*		
C10	https://www.javatpoint.com/computer-organization-and-architecture-tutorial		
D	**Software Tools for Design**		
E	**Recent Developments for Research**	**-**	**-**
F	**Others (Web, Video, Simulation, Notes etc.)**	**-**	**-**
1	https://freevideolectures.com/course/2277/computer-organization		
2	*https://cosmolearning.org/courses/computer-architecture-365/video-lectures/*		

4. Course Prerequisites

Refer to GL01. If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

Students must have learnt the following Courses / Topics with described Content . . .

Modules	Course Code	Course Name	Topic / Description	Sem	Remarks	Blooms Level
1	18EC35	Computer Organization	Software/ Knowledge of Software	3	Have used different software in laboratory	Understand L2
2	18EC35	Computer	No per-requisite to be	3	-	-

		Organization	considered as basics shall be taught as curriculum			
3	18EC35	Computer Organization	No per-requisite to be considered as basics shall be taught as curriculum	3	-	-
4	18EC35	Computer Organization	No per-requisite to be considered as basics shall be taught as curriculum	3	-	-
5	18EC35	Computer Organization	No per-requisite to be considered as basics shall be taught as curriculum	3	-	-

5. Content for Placement, Profession, HE and GATE

The content is not included in this course, but required to meet industry & profession requirements and help students for Placement, GATE, Higher Education, Entrepreneurship, etc. Identifying Area / Content requires experts consultation in the area.

Topics included are like, a. Advanced Topics, b. Recent Developments, c. Certificate Courses, d. Course Projects, e. New Software Tools, f. GATE Topics, g. NPTEL Videos, h. Swayam videos etc.

Modules	Topic / Description	Area	Remarks	Blooms Level
1	Computer Organization and Machine instructions structure	Computer Hardware	Required for Higher Education, Entrepreneurship	L2, L4
2	Input output organization and subroutines and Standard input output interfaces	IO interfacing	Industry & profession requirements	L2
3	Accessing interrupts through different techniques	External hardware interfaces	Industry & profession requirements	L2, L4
4	Memory System and storage devices	Storage devices	Industry	L2,L3
5	Processing unit and Embedded system and large computer system	Embedded Systems	Industry & profession requirements	L2

B. OBE PARAMETERS

1. Course Outcomes

Expected learning outcomes of the course, which will be mapped to POs. Identify a max of 2 Concepts per Module. Write 1 CO per Concept.

Modules	Course Code.#	Course Outcome **At the end of the course, student should be able to . . .**	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
1	18EC35.1	Describe the basic structure of Computer, Performance	04	Operations of	Discussions and	Oral question	L2 Understand

		measurement with CPU clock.		computer	Readings	answers and Explain	
1	18EC35.2	Understand the impact of instruction set architecture on cost-performance of computer design and analyze with various addressing methodologies.	04	Machine instructions structure	Graphic Organizers and Discussion	Analyze and examine and Take home test	L4 Analyzing
2	18EC35.3	Determine the impact of interrupt on input output devices in the process of interaction between various components.	04	Input output organization and interrupts	Lecture and Readings	Questions are convergent and describe in oral	L2 Understand
2	18EC35.4	Understand different kind of input output interfaces available for computer system by demonstrations in lab with disassembling of computer.	04	Standard input output interfaces	Discussion and Readings	Oral and describe	L2 Understand
3	18EC35.5	Determine with the cost-performance issues and design trade-off in designing and constructing a computer processor including memory.	04	Memory System	Readings and Discussion	Student presentations or demonstrations within small groups	L2 Understand
3	18EC35.6	Describes the virtual memory management and secondary storage devices.	04	Storage devices	Graphic Organizers and Discussion	Analyze and Compare	L4 Analyzing
4	18EC35.7	Determine the knowledge of designing a logic circuits and apply to computer system.	04	Arithmetic Operations	Demonstrate problem-solving and process for evaluating	Apply the concepts and use to solve the given problems	L3 Applying L5 Evaluating
4	18EC35.8	Solve the problems in binary representation by using various	04	Different methodolo	Demonstrate	Practice in	L3 Applying

		methods and evaluate with standard circuits.		gies	problem -solving	multiple contexts	
5	18EC35.9	Describe the set of hardware simulators to model a complex processor at the behavioral level.	04	Processing unit	Readings and Discussion	Student presentations	L2 Understand
5	18EC35.10	Determine the current event in the microprocessor research and industry of multiprocessor and embedded systems.	04	Embedded system and large computer system	Readings and Discussion	Student presentations and oral question and answers	L2 Understand
-	**-**	**Total**	**40**	**-**	**-**	**-**	**L2-L4**

2. Course Applications

Write 1 or 2 applications per CO.

Students should be able to employ / apply the course learnings to . . .

Modules	Application Area Compiled from Module Applications.	CO	Level
1	Understand the basic operations of computer system and learn to calculate the performance of CPU with clock.	CO1	L2
2	Understand the way of writing a machine instructions and then analyze the memory allocation methodologies.	CO2	L4
2	Demonstration of input output organization like accessing I/O devices and handling of interrupt events.	CO3	L2
4	Expose different ways of communicating with I/O devices and standard I/O interfaces.	CO4	L2
5	Acquire the knowledge of semiconductor RAM memories, Static memories, Asynchronous DRAMS, Read only memories.	CO5	L2
6	1. Analyze the memory location by having knowledge of various replacement algorithms. 2. Understand the view of virtual memory and secondary storage devices.	CO6	L4
7	Analyze and design the arithmetic operations and Evaluation of logical circuits.	CO7	L3, L5
8	Apply the knowledge gained on various methodologies.	CO8	L3
9	Understand basic processing unit and organization of simple processor with multiple bus organizations.	CO9	L2
10	Demonstration of various embedded system with different devices and their processor chips to gain the importance of life-long learning.	CO10	L2

3. Mapping And Justification

CO – PO Mapping with mapping Level along with justification for each CO-PO pair.

To attain competency required (as defined in POs) in a specified area and the knowledge & ability required to accomplish it.

Modules	Mapping		Mapping Level	Justification for each CO-PO pair	Level
-	**CO**	**PO**	-	**'Area': 'Competency' and 'Knowledge' for specified 'Accomplishment'**	-
1	CO1	PO1	L2	Knowledge of basic structure of computer is needed to build a complex circuits.	L2
1	CO1	PO2	L3	Analyze the performance of the CPU with different processor.	L3
1	CO1	PO3	L4	Processes the performance of the computer to provide solutions for complex problems.	L4
1	CO1	PO4	L3	Analyze the different performance values with standard reference values.	L3
1	CO1	PO7	L2	Understand the impact of different uses of the computer and demonstrate the knowledge to find the solutions.	L2
1	CO1	PO12	L2	Identify new technology to solve various complex problems of the computer.	L2
1	CO2	PO1	L4	Apply the knowledge of computer designing and cost performance for implementing various methodologies for instruction set architecture.	L4
1	CO2	PO2	L2	Identify the proper methodology to over come a various problems of implementing an optimized solution for different instruction sets.	L2
1	CO2	PO3	L4	Processes the complex instruction set architecture to produce the solution that meets the cost-performance of the computer.	L4
1	CO2	PO4	L4	Analyze the cost performance and various addressing methodologies to provide a solution for complex solutions.	L4
1	CO2	PO6	L4	Apply the reasoning for cost performance of various architecture and their uses.	L4
1	CO2	PO7	L2	Understand the impact in societal and find the solutions according to environmental contexts.	L2
1	CO2	PO12	L2	Information acquired from the fundamental of instruction set architecture provides lifelong learning in the context of technological change.	L2
2	CO3	PO1	L5	Apply the evaluation of different hardware components associated with the input-output organization of a computer.	L5
2	CO3	PO2	L4	Analysis of interaction of Input and output with processing unit on various operation.	L4
2	CO3	PO3	L5	Design a system components in such a way that the performance speed should get increase.	L5
2	CO3	PO4	L4	Investigate the different design of a system components and design an optimized solutions.	L4
2	CO3	PO5	L2	Understand the modern tools and technique and apply that to overcome a limitation of complex engineering activities.	L2
2	CO3	PO12	L2	Recognize the need in designing of various input-output devices.	L2

2	CO4	PO1	L2	Knowledge about the various device interfaces of the computer hardware.	L2
2	CO4	PO2	L2	Identify the interfaces available for input and output devices and analyze the different hardware components which uses these interfaces to communicate with processor.	L2
2	CO4	PO3	L4	Processes the system components that meets the appropriate need in performing various operations.	L4
2	CO4	PO4	L4	Analysis of different kind of interfaces which are available for various input output devices.	L4
2	CO4	PO7	L3	Demonstrate the components of the computer by disassembling the system to understand the interfaces.	L3
2	CO4	PO12	L2	Information acquired from the different kind of I/O interfaces which requires lifelong learning in the context of technological change.	L2
3	CO5	PO1	L2	Knowledge of memory storage to give the solution for various complex data storage issues.	L2
3	CO5	PO2	L2	Identify the problems in data storage and analyze the substantiated conclusion using engineering research.	L2
3	CO5	PO3	L6	Design a solution for handling the memory management for storing large amount of data in the system.	L6
3	CO5	PO4	L4	Analysis of available memory spaces in the system in designing and constructing a computer processors.	L4
3	CO5	PO5	L2	Understand the latest techniques and the current need in handling data in memory storage.	L2
3	CO5	PO12	L2	Identify the new technologies to evolve the future use of the memory devices.	L2
3	CO6	PO1	L2	Knowledge about memory management to give implement a virtual memory space in existing device.	L2
3	CO6	PO2	L4	Analyze the problem of memory management and identify the solution by implementing virtual-memory spaces in the same system.	L4
3	CO6	PO3	L4	Design the virtual-memory architecture to manage the available memory space in the storage of large data.	L4
3	CO6	PO7	L2	Understand the impact on current system memory while implementing a virtual memory space in the same system.	L2
3	CO6	PO11	L5	Apply the techniques to create virtual memory spaces to manage projects in multidisciplinary environments.	L5
	CO6	PO12	L 2	Ability to cop up with different methodologies to create a virtual-memory space after learning the memory management schemes.	L 2
4	CO7	PO1	L2	Knowledge about the basic logical gates for designing a complex architecture for system operations.	L2
4	CO7	PO2	L2	Identify the various techniques for designing a logic circuits for different computation.	L2
4	CO7	PO4	L4	Investigate and analyze the circuits based on complexity of the operation.	L4

4	CO7	PO6	L4	Apply the methodologies in a proper manner so that computation should not lead to wrong output.	L4
4	CO7	PO7	L3	Demonstrate the complex calculations solutions by implementing a optimized logic circuits.	L3
4	CO7	PO12	L2	Performing mathematical operation in computer requires the performance issue when it comes to large data so life-long learning is needed in designing optimized logical circuits.	L2
4	CO8	PO1	L2	Knowledge of basic conversions is required to convert complex calculations into machine understand format.	L2
4	CO8	PO2	L2	Identify the optimized method to perform a various mathematical operations in short time.	L2
4	CO8	PO3	L5	Design the optimized circuits for complex problem-solving in the system.	L5
	CO8	PO4	L4	Analyze the various methods for conversion of numerical values into machine understandable form and evaluate the operation with standard circuits.	L4
4	CO8	PO12	L2	Information acquired from the number representation and standard circuits which provides lifelong learning in the context of technological change.	L2
5	CO9	PO1	L2	Knowledge of basic components of computer and instructions execution in the processor.	L2
5	CO9	PO2	L2	Identify the complexity of the current methods and analyze the system operations at a behavioral level of the system.	L2
5	CO9	PO3	L5	Design the set of hardware simulators for complex problems of the processor.	L5
5	CO9	PO5	L2	Select modern simulation tools for developing a optimized solution for processor operation management	L2
5	CO9	PO7	L1	Understand the impact of the hardware devices connected to the system and the need for developing more sustainable technique.	L1
5	CO9	PO12	L2	Recognize the future enhancement needed for solving a various problems in the computer world.	L2
5	CO10	PO1	L2	Knowledge of current events and techniques using with microprocessor to build a solution for complex operations.	L2
5	CO10	PO2	L2	Analyze the various current microprocessor technologies which are using in a different industries and identify the required solution for developing new methodologies.	L2
5	CO10	PO3	L4	Design system components for implementing automatic embedded system for home appliances and more.	L4
5	CO10	PO4	L5	Investigate the current research and analyze the improvements that are needed in the multiprocessing system.	L5
5	CO10	PO5	L4	Understand the current technologies which are available and the limitation to overcome complexity in the system.	L4
5	CO10	PO12	L2	Identify the broadest contexts of technological changes in the multi-core processor and in embedded system.	L2

4. Articulation Matrix

CO - PO Mapping with mapping level for each CO-PO pair, with course average attainment.

-	-	Course Outcomes	Program Outcomes														-
Modules	CO.#	**At the end of the course student should be able to . . .**	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	Level
1	18EC35.1	Describe the basic structure of Computer, Performance measurement with CPU clock.	√	√	√	√			√					√				L2
1	18EC35.2	Understand the impact of instruction set architecture on cost-performance of computer design and analyze with various addressing methodologies.	√	√	√	√		√	√					√				L4
2	18EC35.3	Determine the impact of interrupt on input output devices in the process of interaction between various components.	√	√	√	√	√							√				L2
2	18EC35.4	Understand different kind of input output interfaces available for computer system by demonstrations in lab with disassembling of computer.	√	√	√	√			√					√				L2
3	18EC35.5	Determine with the cost-performance issues and design trade-off in designing and constructing a computer processor including memory.	√	√	√	√	√							√				L2
3	18EC35.6	Describes the virtual memory management and secondary storage devices.	√	√	√				√				√	√				L4
4	18EC35.7	Determine the knowledge of designing a logic circuits and apply to computer system.	√	√		√		√	√					√				L3, L5
4	18EC35.8	Solve the problems in binary representation by using various methods and evaluate with standard circuits.	√	√	√	√			√					√				L3
5	18EC35.9	Describe the set of hardware simulators to model a complex processor at the behavioral	√	√	√		√		√					√				L2

		level.																
5	18EC35.10	Determine the current event in the microprocessor research and industry of multiprocessor and embedded systems.	√	√	√	√	√							√				L2
-	**CS501PC**	**Average attainment (1, 2, or 3)**																**-**
–	*PO, PSO*	*1.Engineering Knowledge; 2.Problem Analysis; 3.Design / Development of Solutions; 4.Conduct Investigations of Complex Problems; 5.Modern Tool Usage; 6.The Engineer and Society; 7.Environment and Sustainability; 8.Ethics; 9.Individual and Teamwork; 10.Communication; 11.Project Management and Finance; 12.Life-long Learning; S1.Software Engineering; S2.Data Base Management; S3.Web Design*																

5. Curricular Gap and Content

Topics & contents not covered (from A.4), but essential for the course to address POs and PSOs.

Modules	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping

6. Content Beyond Syllabus

Topics & contents required (from A.5) not addressed, but help students for Placement, GATE, Higher Education, Entrepreneurship, etc.

Modules	Gap Topic	Area	Actions Planned	Schedule Planned	Resources Person	PO Mapping

C. COURSE ASSESSMENT

1. Course Coverage

Assessment of learning outcomes for Internal and end semester evaluation. Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

Modules	Title	Teach. Hours	No. of question in Exam						CO	Levels
			CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		
1	Basic structure of computer	8	2	–	–	1	1	2	CO1, CO2	L2, L4
2	Input/output Organization	8	2	–	–	1	1	2	CO3, CO4	L2
3	Memory system	8	–	2	–	1	1	2	CO5, CO6	L2, L4
4	Arithmetic operations	8	–	2	–	1	1	2	CO7, CO8	L3,L5
5	Basic processing unit and Embedded system	8	–	–	4	1	1	2	CO9, CO10	L2
-	**Total**	**40**	**4**	**4**	**4**	**5**	**5**	**10**	**-**	**-**

2. Continuous Internal Assessment (CIA)

Assessment of learning outcomes for Internal exams. Blooms Level in last column shall match with A.2.

Modules	Evaluation	Weightage in Marks	CO	Levels
1, 2	CIA Exam – 1	30	CO1 , CO2,CO3 , CO4	L4, L3 , L3 , L4
3, 4	CIA Exam – 2	30	CO5 , CO6,CO7,CO8	L3 , L4 , L4, L2
5	CIA Exam – 3	30	CO9,CO10	L2 , L2
1, 2	Assignment – 1	10	CO1 , CO2,CO3 , CO4	L4, L3 , L3 , L4
3, 4	Assignment – 2	10	CO5 , CO6,CO7,CO8	L3 , L4 , L4, L2
5	Assignment – 3	10	CO9,CO10	L2 , L2
1, 2	Seminar – 1		–	–
3, 4	Seminar – 2		–	–
5	Seminar – 3		–	–
1, 2	Quiz – 1		–	–
3, 4	Quiz – 2		–	–
5	Quiz – 3		–	–
1 – 5	Other Activities – Mini Project	–	–	–
	Final CIA Marks	**40**	**-**	**-**

D1. TEACHING PLAN – 1

Module – 1

Title:	Basic structure of computer	Appr Time:	8 Hrs
a	***Course Outcomes***	–	**Blooms**

-	The student should be able to:	-	**Level**
1	Describe the basic structure of Computer, Performance measurement with CPU clock.	CO1	L2
2	Understand the impact of instruction set architecture on cost-performance of computer design and analyze with various addressing methodologies.	CO2	L4
b	***Course Schedule***	-	-
Class No	**Module Content Covered**	**CO**	**Level**
1	Basic Operational Concepts	CO1	L2
2	Bus Structures	CO1	L2
3	Processor Clock	CO1	L2
4	Basic Performance Equation	CO1	L2
5	CPU Clock Rate	CO1	L2
6	Performance Measurement	CO1	L2
7	Machine Instructions and Programs	CO2	L2
8	Memory Location and Addresses	CO2	L2
9	Memory Operations	CO2	L2
10	Instructions and Instruction Sequencing.	CO2	L4
11	Addressing Modes	CO2	L4
12	Assembly Language	CO2	L4
13	Basic Input and Output Operations	CO2	L2
14	Stacks and Queues, Subroutines	CO2	L2
15	Additional Instructions	CO2	L3
16	Encoding of Machine Instructions	CO2	L2
c	**Application Areas**	**CO**	**Level**
1	Use of the various operations of computer system and learn to calculate the performance of CPU with clock.	CO1	L2
2	Used in addressing a memory location in computer system.	CO2	L4
d	**Review Questions**	-	-
1	With the neat diagram explain different processor register? List the steps needed to execute the machine instruction.	CO1	L2
2	Explain briefly about performance evaluation by using various bench marks.	CO1	L2
3	Draw the basic functional units of a computer.	CO1	L2
4	Explain the operations of stacks and queues.	CO2	L4
5	Discuss about different types of addressing modes.	CO2	L4
6	Explain the operations of stacks and queues.	CO2	L4
7	Give the difference between RISC and CISC.	CO2	L2
8	Write an algorithm for the division of floating point number and illustrate	CO2	L2

	with an example.		
9	Explain BIG-ENDIAN and LITTLE-ENDIAN methods of byte addressing with proper exaple.	CO1	L2
e	**Experiences**	-	-
1			
2			
3			
4			
5			

Module - 2

Title:	Input/output Organization	Appr Time:	8 Hrs
a	***Course Outcomes***	-	**Bloom s**
-	The student should be able to:	-	**Level**
1	Determine the impact of interrupt on input output devices in the process of interaction between various components.	CO3	L2
2	Understand different kind of input output interfaces available for computer system by demonstrations in lab with disassembling of computer.	CO4	L2
b	***Course Schedule***	-	-
Class No	**Module Content Covered**	**CO**	**Level**
17	Input/Output Organization: Accessing I/O Devices	CO3	L2
18	Interrupts - Interrupt Hardware	CO3	L2
19	Enabling and Disabling Interrupts	CO3	L2
20	Handling Multiple Devices	CO3	L2
21	Controlling Device Requests	CO3	L2
22	Exceptions	CO3	L2
23	Direct Memory Access	CO3	L2
24	Buses Interface Circuits	CO4	L2
25	Standard I/O interfaces: PCI BUS, SCSI BUS, USB.	CO4	L2
c	**Application Areas**	**CO**	**Level**
1	Use to Demonstrate of input output organization like accessing I/O devices and handling of interrupt events.	CO3	L2
2	Expose different ways of communicating with I/O devices and standard I/O interfaces.	CO4	L2
d	**Review Questions**	-	-

12	The input status bit in an interface-circuit is cleared as soon as the input data register is read. Why is this important?	CO3	L1
13	What is the difference between a subroutine and an interrupt-service routine?	CO4	L3
14	Consider a computer in which several devices are connected to a common interrupt-request line. Explain how you would arrange for interrupts from device j to be accepted before the execution of the interrupt service routine for device i is completed. Comment in particular on the times at which interrupts must be enabled and disabled at various points in the system.	CO3	L2
15	Consider the daisy chain arrangement. Assume that after a device generates an interrupt-request, it turns off that request as soon as it receives the interrupt acknowledge signal. Is it still necessary to disable interrupts in the processor before entering the interrupt service routine? Why?	CO4	L4
16	Describe the operation of synchronous and asynchronous bus.	CO4	L2
17	Discuss the features of parallel and serial interface techniques.	CO3	L5
18	Describe how a read operation is performed in PCI bus.	CO3	L2
19	Explain how USB operates with split-traffic mode.	CO3	L3
e	**Experiences**	-	-
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E1. CIA EXAM - 1

a. Model Question Paper - 1

Crs Code:	18EC35	Sem:	III	Marks:	30	Time:	75 minutes
Course:	Computer Corganization						

-	-	**Note: Answer any 3 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	With neat diagram, discuss basic operational concepts of a computer.	8	CO1	L1
	b	Write the difference between RISC and CISC processor	8	CO1	L2
	c	Define addressing modes. Explain the following addressing modes with an example for each i) Index addressing ii) Indirect addressing mode iii) Relative addressing mode iv) Auto decrement addressing mode.	9	CO2	L4
2	a	Discuss briefly encoding of machine instruction.	8	CO2	L2

	b	A program contain 1000 instruction out of that 25% instructions requires 4 clock cycles. 40% instruction requires 5 clock cycles and remaining 3 clock cycles for execution. Find the total time required to execute the program running in 1GHz machine.	8	CO2	L4
	c	Explain different Rotate instructions.	7	CO2	L3
	d	Write an ALP program to copy 'N' numbers from array 'A' to array 'B' using direct addresses. (Assume A and B are starting memory locations of an array)	2	CO2	L2
3	a	With neat diagram describe the input output operations.	8	CO3	L1
	b	With neat sketches, explain various methods for handling multiple interrupt requests.	8	CO3	L1
	c	With neat diagram, explain in detail the input interface circuit.	7	CO4	L1
	d	Define Bus Arbitration. Explain any one approach of bus arbitration.	2	CO4	L1
4	a	Write a note on register in DMA interface.	8	CO4	L2
	b	With a block diagram explain how the printer interfaced to processor.	8	CO4	L2
	c	Explain the following with respect to U.S.B i) U.S.B Architecture ii) U.S.B protocols	9	CO4	L1

b. Assignment -1

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	18EC35	Sem:	III	Marks:		Time:	90 - 120 minutes
Course:	Computer Organization						
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	USN	Assignment Description	Marks	CO	Level
1	1KT18EC001	What is bus? Explain single bus and multiple bus structure used to interconnect functional units in computer system.	10	CO1	L2
2	1KT18EC003	Explain how the performance of the computer can measured?	10	CO1	L2
3	1KT18EC004	Explain byte address ability mention the two ways that byte addresses can be assigned across the word with proper example.	10	CO2	L4
4	1KT18EC005	What is an addressing mode? Explain different generic addressing modes with an example for each.	10	CO2	L4
5	1KT18EC008	What are assembler directives? Explain any two directives.	10	CO2	L4
6	1KT18EC009	Explain with neat diagram I/O interface for an input device.	10	CO3	L2
7	1KT18EC010	Explain the following: 1) Interrupt concept 2) interrupt hardware.	10	CO3	L2

8	1KT18EC011	Explain different interrupt Enabling and Disabling methods. List the sequence of events involved in handling an interrupt request from a single device.	10	CO3	L4
9	1KT18EC012	With neat block diagram, Explain different methods of handling multiple I/O devices.	10	CO3	L3
10	1KT18EC013	Define exception. Explain kinds of exceptions?	10	CO3	L2
11	1KT18EC014	What is bus? Explain single bus and multiple bus structure used to interconnect functional units in computer system.	10	CO1	L2
12	1KT18EC015	Explain how the performance of the computer can measured?	10	CO1	L2
13	1KT18EC016	Explain byte address ability mention the two ways that byte addresses can be assigned across the word with proper example.	10	CO2	L4
14	1KT18EC017	What is an addressing mode? Explain different generic addressing modes with an example for each.	10	CO2	L4
15	1KT18EC018	What are assembler directives? Explain any two directives.	10	CO2	L4
16	1KT18EC019	Explain with neat diagram I/O interface for an input device.	10	CO3	L2
17	1KT18EC020	Explain the following: 1) Interrupt concept 2) interrupt hardware.	10	CO3	L2
18	1KT18EC021	Explain different interrupt Enabling and Disabling methods. List the sequence of events involved in handling an interrupt request from a single device.	10	CO3	L4
19	1KT16EC030	With neat block diagram, Explain different methods of handling multiple I/O devices.	10	CO3	L3
20	1KT17EC001	Define exception. Explain kinds of exceptions?	10	CO3	L2
21	DIP	What are assembler directives? Explain any two directives.	10	CO2	L4
22	DIP	Explain with neat diagram I/O interface for an input device.	10	CO3	L2
23	DIP	Explain the following: 1) Interrupt concept 2) interrupt hardware.	10	CO3	L2
24	DIP	Explain different interrupt Enabling and Disabling methods. List the sequence of events involved in handling an interrupt request from a single device.	10	CO3	L4

D2. TEACHING PLAN - 2

Module - 3

Title:	**INTERRUPTS**	Appr Time:	8 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Illustrate the principles for validating the input -output requirements .	CO5	L3

2	Examine the change requirements for interface maintenance .	CO6	L4
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Accessing I/O Devices	CO5	L3
2	Interrupts	CO5	L3
3	Interrupt Hardware	CO5	L3
4	Enabling and Disabling Interrupts	CO5	L3
5	Handling Multiple Devices	CO6	L2
6	Controlling Device Requests.	CO6	L2
7	Direct Memory Access	CO6	L3
8	Direct Memory Access	CO6	L3
c	**Application Areas**	**CO**	**Level**
1	Use to Demonstrate of input output organization like accessing I/O devices and handling of interrupt events.	CO3	L2
2	Expose different ways of communicating with I/O devices and standard I/O interfaces.	CO4	L2
d	**Review Questions**	-	-
12	The input status bit in an interface-circuit is cleared as soon as the input data register is read. Why is this important?	CO3	L1
13	What is the difference between a subroutine and an interrupt-service routine?	CO4	L3
14	Consider a computer in which several devices are connected to a common interrupt-request line. Explain how you would arrange for interrupts from device j to be accepted before the execution of the interrupt service routine for device i is completed. Comment in particular on the times at which interrupts must be enabled and disabled at various points in the system.	CO3	L2
15	Consider the daisy chain arrangement. Assume that after a device generates an interrupt-request, it turns off that request as soon as it receives the interrupt acknowledge signal. Is it still necessary to disable interrupts in the processor before entering the interrupt service routine? Why?	CO4	L4
16	Describe the operation of synchronous and asynchronous bus.	CO4	L2
17	Discuss the features of parallel and serial interface techniques.	CO3	L5
18	Describe how a read operation is performed in PCI bus.	CO3	L2
19	Explain how USB operates with split-traffic mode.	CO3	L3

e	**Experiences**	-	-
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Module - 4

Title:	Memory system	Appr Time:	8 Hrs
a	***Course Outcomes***	-	**Bloom s**
-	The student should be able to:	-	**Level**
1	Determine with the cost-performance issues and design trade-off in designing and constructing a computer processor including memory.	CO7	L2
2	Describes the virtual memory management and secondary storage devices.	CO8	L3
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Memory System: Basic Concepts	CO7	L2
2	Semiconductor RAM Memories	CO7	L2
3	Read Only Memories	CO7	L2
4	Speed, Size, and Cost	CO7	L2
5	Cache Memories – Mapping Functions	CO7	L2
6	Replacement Algorithms	CO7	L2
7	Performance Considerations	CO8	L3
8	Virtual Memories	CO8	L3
9	Secondary Storage.	CO8	L3
c	**Application Areas**	**CO**	**Level**
1	Acquire the knowledge of semiconductor RAM memories, Static memories, Asynchronous DRAMS, Read only memories.	CO7	L2
2	1. Analyze the memory location by having knowledge of various replacement algorithms. 2. Understand the view of virtual memory and secondary storage devices.	CO8	L3
d	**Review Questions**	-	-
1	Consider the dynamic memory cell. Assume that $C = 30$ femtofarads (10^{-15} F) and that leakage current through the transistor is about 0.25 picoamperes (10^{-12} A). The voltage across the capacitor when it is fully charged is 1.5 V. The cell must be refreshed before this voltage drops below 0.9 V. Estimate the minimum refresh rate.	CO7	L2

2	Give a critique of the following statement: "Using a faster processor chip results in a corresponding increase in performance of a computer even if the main-memory speed remains the same."	CO7	L2
3	The cache block size in many computers is in the range of 32 to 128 bytes. What would be the main advantages and disadvantages of making the size of cache blocks larger or smaller?	CO7	L2
4	In a computer with a virtual-memory system, the execution of an instruction may be interrupted by a page fault. What state information has to be saved so that this instruction can be resumed later? Note that bringing a new page into the main-memory involves a DMA transfer, which requires execution of other instructions. Is it simpler to abandon the interrupted instruction and completely re-execute it later? Can this be done?	CO8	L3
5	Magnetic disks are used as the secondary storage for program and data files in most virtual-memory systems. Which disk parameter(s) should influence the choice of page size?	CO8	L3
6	A disk unit has 24 recording surfaces. It has a total of 14,000 cylinders. There is an average of 400 sectors per track. Each sector contains 512 bytes of data. i) What is the maximum number of bytes that can be stored in this unit ? ii) What is the data-transfer rate in bytes per second at a rotational speed of 7200 rpm? iii) Using a 32-bit word, suggest a suitable scheme for specifying the disk address.	CO8	L3
7	Discuss the main features of SDRAM with a neat diagarm.	CO8	L3
e	**Experiences**	-	-
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E2. CIA EXAM - 2

a. Model Question Paper - 2

Crs Code:	18EC35	Sem:	3	Marks:	30	Time:	80 minutes
Course:	Computer organisation						

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Explain the Interrupt Hardware.	5	L2	8

	b	Explain the Enabling and Disabling Interrupts.	5	L2	8
	c	Explain Direct Memory Access.	6	L2	9
		OR			
2	a	Explain the different techniques of IO mechanism.	5	L2	8
	b	Explain the different types of interrupt schemes.	6	L2	8
	c	Explain Controlling Device Requests.	6	L2	9
3	a	Explain Internal organization of memory chips.	7	L2	8
	b	Explain Asynchronous DRAMs.	7	L2	8
	c	Explain Static memories.	8	L2	9
		OR			
4	a	Explain Read Only Memories.	7	L2	8
	b	Explain basic concepts of memory.	7	L2	8
	c	Explain Semiconductor RAM Memories.	8	L2	9

b. Assignment - 2

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	18EC35	Sem:	III	Marks:		Time:	90 - 120 minutes
Course:	Computer Organization						
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	USN	Assignment Description	Marks	CO	Level
1	1KT18EC001	Explain connection between memory and processor with memory read and write operations?	10	CO5	L2
2	1KT18EC003	Draw the organization of 1Kx1 memory cell and explain its working.	10	CO5	L2
3	1KT18EC004	Write briefly about read only memories and Flash memory's.	10	CO5	L4
4	1KT18EC005	Draw the organization of a 16x memory chip and explain its working.	10	CO6	L2
5	1KT18EC008	What is refreshing? Explain the concept of refreshing in dynamic memory?	10	CO6	L2
6	1KT18EC009	With a neat diagram explain the virtual memory organization.	10	CO7	L3
7	1KT18EC010	What is virtual memory? With a diagram explain how virtual memory address is translated.	10	CO7	L2
8	1KT18EC011	With a neat diagram explain the translation of virtual address to a physical address?	10	CO7	L4
9	1KT18EC012	Explain the 4-bit carry look ahead adder.	10	CO8	L3
10	1KT18EC013	Design a logic circuit to perform addition and subtraction of two 'n' numbers X and Y.	10	CO8	L2
11	1KT18EC014	Explain connection between memory and processor with memory read and write operations?	10	CO5	L2

12	1KT18EC015	Draw the organization of 1Kx1 memory cell and explain its working.	10	CO5	L2
13	1KT18EC016	Write briefly about read only memories and Flash memory's.	10	CO5	L4
14	1KT18EC017	Draw the organization of a 16x memory chip and explain its working.	10	CO6	L2
15	1KT18EC018	What is refreshing? Explain the concept of refreshing in dynamic memory?	10	CO6	L2
16	1KT18EC019	With a neat diagram explain the virtual memory organization.	10	CO7	L3
17	1KT18EC020	What is virtual memory? With a diagram explain how virtual memory address is translated.	10	CO7	L2
18	1KT18EC021	With a neat diagram explain the translation of virtual address to a physical address?	10	CO7	L4
19	1KT16EC030	Explain the 4-bit carry look ahead adder.	10	CO8	L3
20	1KT17EC001	Design a logic circuit to perform addition and subtraction of two 'n' numbers X and Y.	10	CO8	L2
21	DIP	With a neat diagram explain the virtual memory organization.	10	CO7	L3
22	DIP	What is virtual memory? With a diagram explain how virtual memory address is translated.	10	CO7	L2
23	DIP	With a neat diagram explain the translation of virtual address to a physical address?	10	CO7	L4
24	DIP	Explain the 4-bit carry look ahead adder.	10	CO8	L3

D3. TEACHING PLAN - 3

Module - 5

Title:	Basic processing unit and Embedded system	Appr Time:	8 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Describe the set of hardware simulators to model a complex processor at the behavioral level.	CO9	L2
2	Determine the current event in the microprocessor research and industry	CO10	L2

	of multiprocessor and embedded systems.		
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Basic Processing Unit: Some Fundamental Concepts	CO9	L2
2	Execution of a Complete Instruction	CO9	L2
3	Multiple Bus Organization	CO9	L2
4	Hard-wired Control	CO9	L2
5	Micro programmed Control	CO9	L2
6	Pipe lining	CO9	L2
7	Embedded Systems and Large Computer Systems: Basic Concepts of pipe lining	CO10	L2
8	Examples of Embedded Systems	CO10	L2
9	Processor chips for embedded applications	CO10	L2
10	Simple Micro controller	CO10	L2
11	The structure of General-Purpose Multiprocessors	CO10	L2
c	**Application Areas**	**CO**	**Level**
1	Understand basic processing unit and organization of simple processor with multiple bus organizations.	CO9	L2
2	Demonstration of various embedded system with different devices and their processor chips to gain the importance of life-long learning.	CO10	L2
d	**Review Questions**	-	-
1	Why is the Wait-for-memory-function-completed step needed for reading from or writing to the main memory?	CO10	L1
2	For the single bus organization, write the complete control sequence for the instruction: Move (R1), R1	CO10	L3
3	Write the sequence of control steps required for the single bus organization in each of the following instructions: Add the immediate number NUM to register R1. Add the contents of memory-location NUM to register R1. Add the contents of the memory-location whose address is at memory-location NUM to register R1. Assume that each instruction consists of two words. The first word specifies the operation andN the addressing mode, and the second word contains the number NUM	CO9	L2
4	Show the control steps for the Branch on Negative instruction for a processor with three-bus organization of the data path	CO9	L4
5	With block diagram, explain NUMA multiprocessor.	CO10	L2
6	Write a short not on home telemetry.	CO10	L2
7	With block diagram, explain operation of counter/timer.	CO10	L2

8	With block diagram, explain operation of microcontroller chips.	CO10	L3
9	With block diagram, explain serial I/O interface. Also, explain serial interface register	CO9	L4
10	Draw and explain multiple bus organization along with its advantages.	CO10	L3
11	Write down the control sequence for the instruction Add (R3) , R1 for single bus organization	CO10	L3
e	**Experiences**	-	-
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E3. CIA EXAM - 3

a. Model Question Paper - 3

Crs Code:	18EC35	Sem:	III	Marks:	30	Time:	75 minutes
Course:	Computer Organization						

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Briefly explain any two mapping function used in cache memory.	12	CO7	L2
	b	With a neat diagram explain the internal organization of memory chip(2M*8 and dynamic memory chip)	13	CO7	L2
2	a	Explain the following: i) Hit rate and miss penalty. ii) Memory Latency. iii) Memory Bandwidth. iv) Virtual memory organization.	8	CO8	L2
	b	What is virtual memory? With a diagram explain how virtual memory address translation takes place.	8	CO8	L2
	c	Differentiate between hardwired control and micro program control.	9	CO8	L2
3	a	With a figure explain Single Bus Organization of data path inside a processor.	12	CO9	L2
	b	Write the sequence of control steps required to execute the following instruction ADD (R3), R1.	13	CO9	L3
4	a	With a block diagram explain the working of microwave oven in an embedded system.	12	CO10	L2
	b	Draw and explain multiple bus organization of CPU. And write the control sequence for the instruction ADD R4,R5,R6 for multiple bus organization.	13	CO9	L3

b. Assignment - 3

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	18EC35	Sem:	III	Marks:	10 / 10	Time:	90 - 120 minutes
Course:	Computer Organization						
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	USN	Assignment Description	Marks	CO	Level
1	1KT18EC001	Write down the control sequence for the instruction Add R4, R5, R6 for three-bus organization.	10	CO9	L2
2	1KT18EC003	With a neat sketches explain the organization of a micro programmed control unit.?	10	CO9	L3
3	1KT18EC004	With a diagram explain typical single bus processor data path?	10	CO10	L4
4	1KT18EC005	Differentials hardwired and micro programmed control unit?	10	CO10	L3
5	1KT18EC008	Explain the process of fetching a word from memory with diagram?	10	CO10	L3
6	1KT18EC009	With a block diagram explain the working of microwave oven in an embedded system.	10	CO10	L2
7	1KT18EC010	Draw and explain multiple bus organization of CPU. And write the control sequence for the instruction ADD R4,R5,R6 for multiple bus organization.	10	CO9	L3
8	1KT18EC011	Write down the control sequence for the instruction Add R4, R5, R6 for three-bus organization.	10	CO9	L2
9	1KT18EC012	With a neat sketches explain the organization of a micro programmed control unit.?	10	CO9	L3
10	1KT18EC013	With a diagram explain typical single bus processor data path?	10	CO10	L4
11	1KT18EC014	Differentials hardwired and micro programmed control unit?	10	CO10	L3
12	1KT18EC015	Explain the process of fetching a word from memory with diagram?	10	CO10	L3
13	1KT18EC016	With a block diagram explain the working of microwave oven in an embedded system.	10	CO10	L2
14	1KT18EC017	Draw and explain multiple bus organization of CPU. And write the control sequence for the instruction ADD R4,R5,R6 for multiple bus organization.	10	CO9	L3
15	1KT18EC018	Write down the control sequence for the instruction Add R4, R5, R6 for three-bus organization.	10	CO9	L2
16	1KT18EC019	With a neat sketches explain the organization of a micro programmed control unit.?	10	CO9	L3
17	1KT18EC020	With a diagram explain typical single bus processor data path?	10	CO10	L4

18	1KT18EC021	Differentials hardwired and micro programmed control unit?	10	CO10	L3
19	1KT16EC030	Explain the process of fetching a word from memory with diagram?	10	CO10	L3
20	1KT17EC001	With a block diagram explain the working of microwave oven in an embedded system.	10	CO10	L2
21	DIP	Draw and explain multiple bus organization of CPU. And write the control sequence for the instruction ADD R4,R5,R6 for multiple bus organization.	10	CO9	L3
22	DIP	With a block diagram explain the working of microwave oven in an embedded system.	10	CO9	L2
23	DIP	Draw and explain multiple bus organization of CPU. And write the control sequence for the instruction ADD R4,R5,R6 for multiple bus organization.	10	CO9	L3
24	DIP	With a diagram explain typical single bus processor data path?	10	CO10	L4

F. EXAM PREPARATION

1. University Model Question Paper

Course:	Computer Organization					Month / Year	June /2018
Crs Code:	18EC35	Sem:	III	Marks:	100	Time:	180 minutes

-	Note	Answer all FIVE full questions. All questions carry equal marks.	Marks	CO	Level
1	a	Define Addressing Mode. Give the details of different addressing modes.	10	CO1	L2
	b	Describe the basic operational concepts between the processor and memory.	10	CO2	L2
		OR			
2	a	What is Subroutine? How to pass parameters to subroutines? Illustrate with an example	10	CO1	L2
	b	How to encode assembly instructions into 32-bit words? Explain with examples.	10	CO2	L4
3	a	Define Bus Arbitration. With diagrams, explain the centralized bus arbitration mechanism.	10	C03	L2
	b	With the help of timing diagram, briefly discuss the main phases of SCSI bus involved in its operation.	10	CO4	L2
		OR			
4	a	With neat diagrams, explain how to interface printer to the processor.	10	CO3	L2
	b	Explain the following methods of handling interrupts from multiple devices. i) Interrupt nesting/priority structure	10	CO4	L2

		ii) Daisy chain method.			
5	a	Describe how to translate virtual address into physical address with diagram.	10	CO5	L2
	b	Draw and explain the internal organisation of 2M x 8 asynchronous DRAM chip.	10	CO6	L2
		OR			
6	a	Describe any two mapping functions in cache.	10	CO5	L2
	b	Describe the principles of magnetic disk.	10	CO6	L2
7	a	form the operations on 5 — bit signed numbers using 2's complement system. Also indicate whether overflow has occurred. i) (-10) + (-13) ii) (-10) — (-13) iii) (-2) + (-9).	10	CO7	L3
	b	Perform the multiplication of 13 and -6 using Booth algorithm and Bit- pair recording method.	10	C08	L3
		OR			
8	a	Perform the restoring division for 8/3 by showing all the steps	10	CO7	L3
	b	Explain the logic diagram of 4 — bit carry look ahead adder and its operations.	10	CO8	L2
9	a	Draw and explain multiple bus organization along with its advantages.	10	CO9	L2
	b	Write down the control sequence for the instruction Add (R3) , R1 for single bus organization	10	CO10	L3
		OR			
10	a	With block diagram, explain the general requirements and working of digital camera.	10	CO9	L2
	b	Write the control sequence for an unconditional branch instruction.	10	CO10	L2

2. SEE Important Questions

Course:	Computer Organization					Month / Year	June /2018	
Crs Code:	18EC35	Sem:	III	Marks:	100	Time:	180 minutes	
	Note	Answer all FIVE full questions. All questions carry equal marks.				-	-	
Module	Qno.	Important Question				**Marks**	**CO**	**Year**
1	1	With neat diagram explain simple I/O operations involving in keyboard and display device.				5	CO1	2018

	2	Define subroutine. Explain subroutine linkage using a link register and stack frame.	6	CO1	2017
	3	Explain different parameter passing technique with usage of stack in nested subroutine calls.	7	CO1	2015
	4	Explain different shift and rotate instructions with proper examples.	7	CO2	2015
	5	Explain encoding of machine instruction into 32-bit word.	8	CO2	2016
2	1	What is necessity of DMA controller? Explain (1) Cycle stealing (2) Burst mode.	6	CO3	2017
	2	Show the possible register configurations in DMA interface, Explain direct memory access(DMA)	7	CO3	2018
	3	What is necessity of BUS Arbitration? Explain different methods of bus arbitration.	6	CO4	2017
	4	Define BUS? Explain with neat detailed timing diagram for the input transfer using multiple clock cycle of synchronous Bus?	7	CO4	2016
	5	Explain with neat detailed timing diagram for handshake control of data transfer during an output operation.	7	CO4	2015
3	1	Explain the working of 16MB DRAM chip configured as 1M*16 (2M*8) memory chip.	5	CO5	2015
	2	Define: i) Memory latency ii) Memory bandwidth iii) Hit rate iv) Miss penalty.	8	CO5	2016
	3	With diagram explain different types of memory's with speed, cost and size.	6	CO5	2017
	4	Define cache memory? Explain different cache mapping functions.	6	CO5	2018
	5	Explain the features of memory design that leads to improved performance of computer.	6	CO6	2015
4	1	Given A=10101 and B=00100, Perform A/B using restoring division algorithms.	5	Co7	2016
	2	Perform signed multiplication of numbers (-12) and (-11) using Booth's algorithm.	7	CO7	2016
	3	Design 4-bit carry look ahead logic and explain how it is faster than 4-bit ripple adder.	8	CO7	2017
	4	Explain normalization, excess-exponent and special values with respect to IEEE floating point representation.	5	CO8	2018
	5	Perform the following operations on the 5-bit signed numbers using 2's compliment representation system. Also indicate whether overflow has occurred i) (-10) + (-13) ii) (-10) - (+4) iii) (-3) + (-8) iv) (-10) - (+7)	8	CO8	2014
5	1	Write and explain the control sequences for the execution of an unconditional branch instruction.	8	CO9	2015
	2	Draw and explain the multi-bus organization of the data path inside	6	CO9	2016

		a processor?			
	3	What is embedded system? Explain with examples.	7	CO10	2015
	4	Explain with neat diagram structure of general purpose multiprocessor?	8	CO10	2018
	5	Explain Agile Manifesto.	10	CO9	L2

G. Content to Course Outcomes

1. TLPA Parameters

Table 1: TLPA – Example Course

Module-#	Course Content or Syllabus (Split module content into 2 parts which have similar concepts)	Content Teaching Hours	Blooms' Learning Levels for Content	Final Blooms' Level	Identified Action Verbs for Learning	Instruction Methods for Learning	Assessment Methods to Measure Learning
A	*B*	*C*	*D*	*E*	*F*	*G*	*H*
1	Describe the basic structure of Computer, Performance measurement with CPU clock.	4	L4 Analyze	L4 Analyze	– Understand – Explore	Lecture	Slip test
1	Understand the impact of instruction set architecture on cost-performance of computer design and analyze with various addressing methodologies.	4	L3 Apply	L3 Apply	–Identify –	Explanation	Q & A
2	Determine the impact of interrupt on input output devices in the process of interaction between various components.	4	L3 Apply	L3 Apply	– Interpret –	Description	Q & A
2	Understand different kind of input output interfaces available for computer system by demonstrations in lab with disassembling of computer.	4	L4 Analyze	L4 Analyze	– Compare –	Explanation	Q & A
3	Determine with the cost-performance issues and design trade-off in designing and constructing a computer processor including memory.	4	L3 Apply	L3 Apply	– Illustrate –	Examine	Focused on analyzing / compare
3	Describes the virtual memory management and secondary storage devices.	4	L4 Analyze	L4 Analyze	– Examine –	Description	Q & A
4	Determine the knowledge of designing a logic circuits and apply to computer system.	4	L4 Analyze	L4 Analyze	–Analyze –	Explanation	Slip test
4	Solve the problems in binary	4	L2	L2	–Identify	Descript	Q & A

	representation by using various methods and evaluate with standard circuits.		Understand	Understand	-	ion	
5	Describe the set of hardware simulators to model a complex processor at the behavioral level.	4	L2 Understand	L2 Understand	- Understand -	Develop	Q & A
5	Determine the current event in the microprocessor research and industry of multiprocessor and embedded systems.	4	L2 Understand	L2 Understand	-Explain -	Description	Q & A

2. Concepts and Outcomes:

Table 2: Concept to Outcome – Example Course

Module-#	Learning or Outcome from study of the Content or Syllabus	Identified Concepts from Content	Final Concept	Concept Justification (What all Learning Happened from the study of Content / Syllabus. A short word for learning or outcome)	CO Components (1.Action Verb, 2.Knowledge, 3.Condition / Methodology, 4.Benchmark)	Course Outcome **Student Should be able to ...**
A	*I*	*J*	*K*	*L*	*M*	*N*
1	Describe the basic structure of Computer, Performance measurement with CPU clock.	Operations of computer	Operations of computer	Process activities	-Explore -software system, component or process -system models -realistic constraints.	Explore the various types of system
1	Understand the impact of instruction set architecture on cost-performance of computer design and	Machine instructions structure	Machine instructions structure	Requirement Analysis	-Identify -requirements for development, -Requirements Engineering Processes.	Identify the development requirements

	analyze with various addressing methodologies.					
2	Determine the impact of interrupt on input output devices in the process of interaction between various components.	Input output organization and interrupts	Input output organization and interrupts	Development models	-Interpret -Analysis of requirements -appropriate design	Interpret the usage of suitable models
2	Understand different kind of input output interfaces available for computer system by demonstrations in lab with disassembling of computer.	Standard input output interfaces	Standard input output interfaces	Design techniques	-Compare - development -Design techniques,	Compare various design techniques for development.
3	Determine with the cost-performance issues and design trade-off in designing and constructing a computer processor including memory.	Memory System	Memory System	Levels of software testing	-Illustrate - requirements and maintenance practices -Validating	Illustrate the principles for validating the requirements .
3	Describes	Storage	Storage	Evolution process	-Examine	Examine the

	the virtual memory management and secondary storage devices.	devices	devices		- Maintenance -Change requirement	change requirements for maintenance .
4	Determine the knowledge of designing a logic circuits and apply to computer system.	Arithmetic Operations	Arithmetic Operations	Development panning	-Analyze - project management -quality assurance procedures	Analyze the plans
4	Solve the problems in binary representation by using various methods and evaluate with standard circuits.	Different methodologies	Different methodologies	Quality assurance procedures	-Identify - development process -Quality assurance procedures	Identify the quality assurance procedures
5	Describe the set of hardware simulators to model a complex processor at the behavioral level.	Processing unit	Processing unit	Agile methods for software development	-Understand	Understand the importance of agile project management
5	Determine the current event in the microprocessor research and industry of multiprocessor and	Embedded system and large computer system	Embedded system and large computer system	Agile methods for software development	-Explain, development -methods	Explain the method for Development .

	embedded systems.					